Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended): An electrostatic discharge protection circuit comprising:

an npn Darlington circuit comprising [[a]] an input end and an output end~~, the output end of the npn Darlington circuit being grounded~~; and

an N-type channel metal-oxide semiconductor (NMOS) transistor, a drain of the NMOS transistor connected to the input end of the npn Darlington circuit, a source of the NMOS transistor connected to a control end of the npn Darlington circuit, a gate of the NMOS transistor connected to the output end of the npn Darlington circuit.

Claim 2 (original): The electrostatic discharge protection circuit of claim 1 wherein the npn Darlington circuit further comprises two npn-type bipolar junction transistors (BJTs), each npn BJT comprising an N+ buried layer, a P well formed on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises an N+ buried layer, a P well formed on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and two N+ nodes formed in a top side of the P well.

Claim 3 (original): The electrostatic discharge protection circuit of claim 2 wherein the two BJTs and the NMOS transistor are formed on a P-substrate, and the N wells of the two npn BJTs and the NMOS transistor are used to isolate the P wells and the P-substrate.

Claim 4 (original): The electrostatic discharge protection circuit of claim 3 further comprising a P-epi layer formed on the P-substrate, and wherein the N wells of the two npn BJTs and the NMOS transistor are formed on the P-epi layer.

Claim 5 (original): The electrostatic discharge protection circuit of claim 3 further comprising an N-epi layer formed on the P-substrate, and the N wells of the two npn BJTs and the NMOS transistor are formed on the N-epi layer.

Claim 6 (original): The electrostatic discharge protection circuit of claim 3 wherein the circuit is manufactured by a BiCMOS process.

Claim 7 (original): The electrostatic discharge protection circuit of claim 1 wherein the npn Darlington circuit further comprises two npn BJTs, each npn BJT comprising a deep N well, a P well formed on the deep N well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises a deep N well, a P well formed on the N well, and two N+ nodes formed in a top side of the P well.

Claim 8 (original): The electrostatic discharge protection circuit of claim 7 wherein the two BJTs and the NMOS transistor are formed on a P-substrate, and the deep N wells of the two npn BJTs and the NMOS transistor are used to isolate the P wells and the P-substrate.

Claim 9 (original): The electrostatic discharge protection circuit of claim 8 wherein the circuit is manufactured by a CMOS process.

Claim 10 (original):The electrostatic discharge protection circuit of claim 1 wherein the input end of the npn Darlington circuit is connected to an input end of another circuit.

Claim 11 (original):The electrostatic discharge protection circuit of claim 1 wherein the

input end of the npn Darlington circuit is connected to a voltage source.

Claim 12 (original):The electrostatic discharge protection circuit of claim 1 further comprising:

a pnp Darlington circuit, an input end of the pnp Darlington circuit connected to the input end of the npn Darlington circuit, an output end of the pnp Darlington circuit connected to a voltage source; and

a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the PMOS transistor connected to the input end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp Darlington circuit, a gate of the PMOS transistor connected to the output end of the pnp Darlington circuit.

Claim 13 (new): An electrostatic discharge protection circuit comprising:

a pnp Darlington circuit comprising an input end and an output end; and

a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the PMOS transistor connected to the output end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp Darlington circuit, a gate of the PMOS transistor connected to the input end of the pnp Darlington circuit.